Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**ANODE**

**.018” X .017”**

**.031”**

**.031”**

**Top Material: Au**

**Backside Material: Au**

**Bond Pad Size: .017” X .071”**

**Backside Potential: CATHODE**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .031” X .031” DATE: 3/25/16**

**MFG: SUSSEX THICKNESS .010” P/N: SZ.75-24-40-.25E**

**DG 10.1.2**

#### Rev B, 7/1